# ON-CHIP DIFFERENTIAL MULTI-LAYER INDUCTOR

## ABSTRACT OF THE DISCLOSURE

An on-chip differential multi-layer inductor includes a 1st partial winding on a 1st layer, a 2nd partial winding on the 1st layer, a 3rd partial winding on a 2nd layer, a 4th partial winding on the 2nd layer, and an interconnecting structure. The 1st and 2nd partial windings on the 1st layer are operably coupled to receive a differential input signal. The 3rd and 4th partial windings on the 2nd layer are each operably coupled to a center tap. The interconnecting structure couples the 1st, 2nd, 3rd and 4th partial windings such that the 1st and 3rd partial windings form a winding that is symmetrical about the center tap with a winding formed by the 2nd and 4th partial windings. By designing the on-chip differential multi-layer inductor to have a desired inductance value, a desired Q factor, and a desired operating rate, a desired resonant frequency and corresponding desired capacitance value can be determined. Having determined the electrical parameters of the multi layer established, the geometric shapes of the windings, number of windings, number of layers to support the inductor, and the interconnecting structure may be determined.